IN THE DRAWINGS

The Examiner objected to FIG. 3 for failure to show every feature of the invention specified in the claims. The Examiner's permission is requested to make the following changes to the drawings to correspond with the specification as required by MPEP §608.01(g). Applicants have submitted replacement figures reflecting the corrections made to overcome the Examiner's objections. A copy of the drawings marked "Annotated" showing the changes in red along with a "Replacement Sheet" which complies with 37 CFR 1.84 have been submitted herewith. No new matter has been added.

REMARKS/ARGUMENTS

Applicants have studied the Final Office Action dated February 22, 2005. No new matter has been added. It is submitted that the application is in condition for allowance. Applicants have amended claims 1 and 9-11. By virtue of this amendment, claims 1-14 are pending. Reconsideration and further examination of the pending claims in view of the above amendments and the following remarks is respectfully requested. In the Final Office Action, the Examiner:

(1) Objected to Figure 3 for failure to show every feature of the invention specified in the claims;

(2-3) Rejected claims 1-14 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; and

(4-5) Rejected claims 1-14 under 35 U.S.C. §102(b) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798).

Telephone Conference

The Applicants would like to thank Examiner Nguyen for the teleconference on March 2, 2005, where matters regarding the clarification of FIG. 3 and the independent claims of the present invention were discussed. FIG. 3 along with the accompanying text in the specification as originally filed has the correct labels identifying the transistors as being either P-channel or N-channel. For further clarification, the Applicants have amended FIG. 3 to include industry standard symbols identifying P-channel transistors. Additionally, claims 1 and 9-11 have been amended to further clarify the present invention. Applicants believe that in view of the amended FIG. 3 and the clarified amended claims 1 and 9-11, claims 1-14 are in allowable form as per the previous Amendment dated January 3, 2005.

(1) Objection to Figures

As noted above, the Examiner objected to Figure 3 for failure to show every feature of the invention specified in the claims. Applicants have submitted a replacement figure reflecting the corrections made to overcome the Examiner's objections. No new matter was added. The Applicants respectfully request that the Examiner's objection to the drawings be withdrawn.

(2-3) Rejection under 35 U.S.C. §112, second paragraph

As noted above, the Examiner rejected claims 1-14 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Applicants have carefully amended claims 1-6. 9-13 as suggested by the Examiner. Support for this amendment may be found in the specification as originally filed, see for example FIG. 3; pages 6-7. No new matter has been added.

Amended claims 1 and 9-11 now more clearly and affirmatively point out that each delay stage includes uniform minimum channel length transistors of two different types of conductivity. Therefore, the remaining elements of independent claims 1 and 9-11 do not contradict each other as stated by the Examiner. Accordingly, Applicants submit that claims 1 and 9-11 are allowable, and the Examiner's rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

Claims 7-8 depend from claims 1. Since dependent claims recite all of the limitations of the independent claim; the Applicants submit that claims 7-8 are also allowable, and the Examiner's rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

(4-5) Rejection under 35 U.S.C. §102(b) as being anticipated by Sato et al

As noted above, the Examiner rejected claims 1-14 under 35 U.S.C. §102(b) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798). Independent claims 1 and 9-11 have been amended to further clarify the present invention and distinguish over Sato. The present invention, as recited for amended claims 1 and 9-11, now recites, among other things:

> wherein each delay stage includes **a stack of uniform minimum channel length transistors** with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type;
>
> wherein the use of uniform minimum channel length transistors provides uniform tolerance variations across a circuit

The emphasis of the Sato reference is a synchronous semiconductor memory device that is operable in a snooze mode. See Sato Abstract and col. 2, lines 61-67 to col. 3, lines 1-17. The Examiner directs Applicants to FIG. 14A of Sato, wherein Sato discloses a delay element used in an internal snooze mode signal generating portion. See Sato col. 13, lines 14-34 and col. 14, lines 32-33. Sato discloses that the gate circuits of the delay element have the same structure and each include a plurality of (three) p-channel MOS transistors and a plurality of (three) n-channel MOS transistors. The gates of a plurality of MOS transistors are connected to an input node and the gate capacitances of these transistors in combination increase the capacitance of the input node. The p-channel MOS transistors are connected in series between a power supply node and an output node. Consequently, a resistance between the power supply node and output node increases so that a capability of supplying a current to the output node decreases, resulting in a slow rising of its potential.

In contrast, as now recited for amended claims 1, 9-10, and similarly for amended Claim 11, the presently claimed invention recites "wherein each delay stage includes **a stack of uniform minimum channel length transistors** with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type" and

"wherein the use of uniform minimum channel length transistors provides uniform tolerance variations a circuit."

The use of minimum channel length transistors as recited in the present invention provides many advantages. For example, parametric tracking is increased and standard modeling techniques can be used. Also, the present invention uses stacks of minimum channel length devices and not various channel length devices, thereby resulting in a similar stage delay while eliminating the need for extended channel length devices. The use of minimum channel length transistors provides uniform tolerance variations across the circuit. Another advantage of the present invention is that the minimum channel length transistor, as recited by the present invention, is physically smaller than conventional transistors. Another advantage is that the delay element of the present invention improves production, such as increased chip yield.

Sato, on the other hand, does not teach, anticipate, or even suggest **a stack of uniform minimum channel length transistors** with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type or that the use of uniform minimum channel length transistors provides uniform tolerance variations a circuit a circuit, as recited by amended claims 1 and 9-11.
In fact, Sato is completely silent on both matters. The Examiner directs Applicants to FIG. 14A of Sato. However, no where in the figures or the Specification does Sato disclose that minimum channel length transistors are used in the delay element. Careful reading of Sato does not teach or suggest that the transistors P1-P3 and N1-N3 are uniform minimum channel length transistors. Additionally, Sato is directed towards the post-production stage of the circuit and is not concerned with providing uniform tolerance variations a circuit across a circuit. Accordingly, independent claims 1 and 9-11 distinguish over Sato for at least this reason.

For the foregoing reasons, independent claims 1 and 9-11 as amended distinguish over Sato. Claims 2-8, and 12-14 depend from independent Claims 1 and 11 respectively. Since dependent claims contain all the limitations of the independent claims, claims 2-8,

and 12-14 distinguish over Sato, as well, and the Examiner's rejection should be withdrawn.

The Examiner cites 35 U.S.C. § 102(b) and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected claims as being anticipated by Sato.[1] The elements in independent claims 1 and 9-11 of "**a stack of uniform minimum channel length transistors** with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type," the rejection of claims 1 and 9-11 under 35 U.S.C. 102(b) as being anticipated by Sato has been overcome. The Examiner should withdraw the rejection of these claims. Accordingly, the present invention distinguishes over Sato for at least this reason as well. The Applicants respectfully submit that the Examiner's rejection under 35 U.S.C. § 102(b) has been overcome.

CONCLUSION

The foregoing is submitted as full and complete response to the Official Action mailed February 22, 2005, and it is submitted that claims 1-14 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of claims 1-14 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

---

[1] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

Applicants acknowledge the continuing duty of candor and good faith to disclosure of information known to be material to the examination of this application. In accordance with 37 CFR §§ 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

The present application, after entry of this amendment, comprises fourteen (14) claims, including four (4) independent claims. Applicants have previously paid for fourteen (14) claims including four (4) independent claims. Applicants, therefore, believe that a fee for claims amendment is currently not due.

Applicants respectfully submit that all of the grounds for rejection stated in the Examiner's Office Action have been overcome, and that all claims in the application are allowable. No new matter has been added. It is believed that the application is now in condition for allowance, which allowance is respectfully requested.

PLEASE CALL the undersigned if that would expedite the prosecution of this application.

Respectfully Submitted,

Date: May 23, 2005

By: _____

Attorney for the Applicants
Jon A. Gibbons
(Reg. No. 37,333)

Customer Number 23334
Fleit, Kain, Gibbons, Gutman,
Bongini & Bianco P.L.
One Boca Commerce Center, Suite 111
551 N.W. 77th Street
Boca Raton, FL 33487
Telephone No.: (561) 989-9811
Facsimile No.: (561) 989-9812

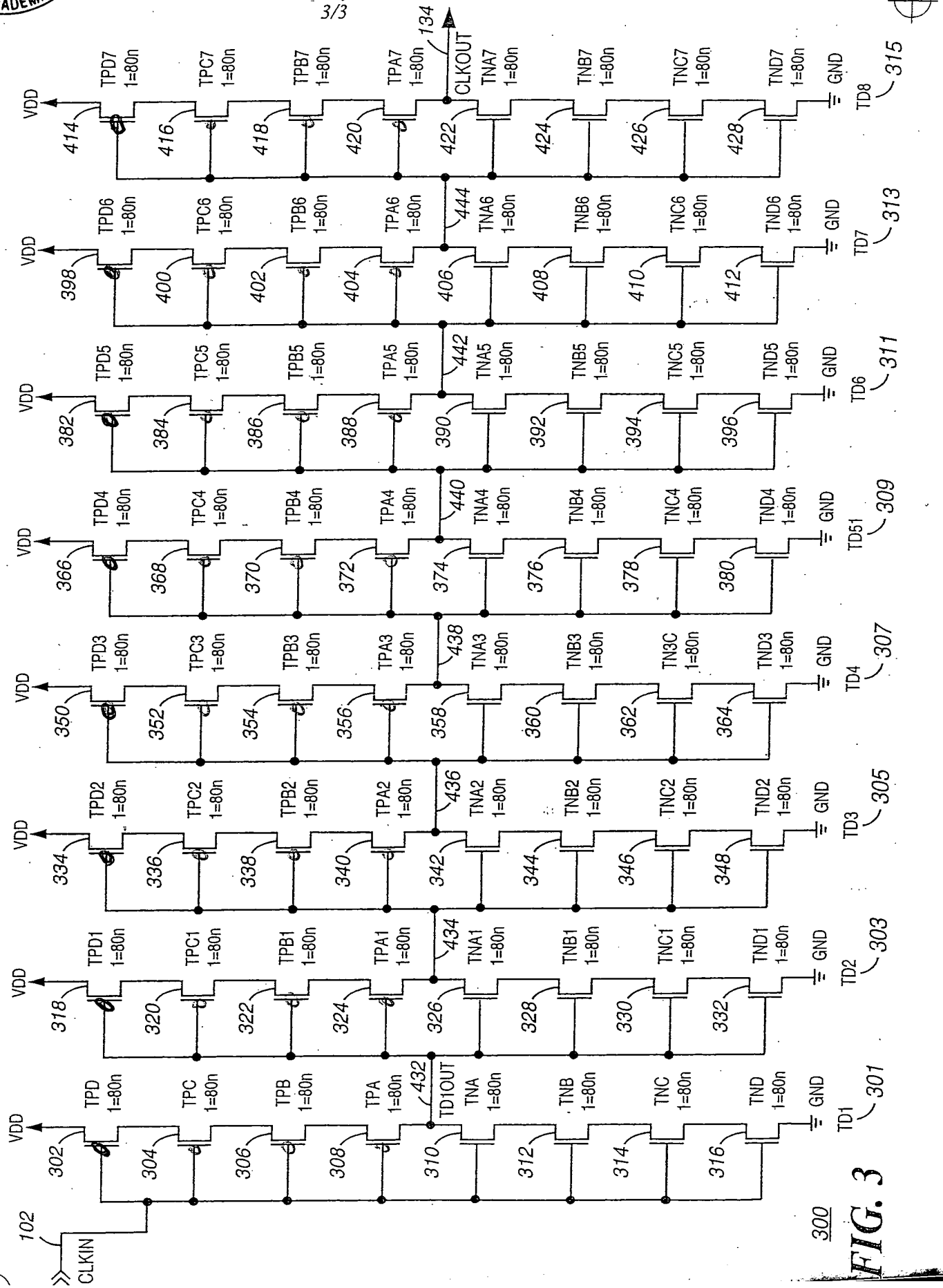

FIG. 3